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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
BRITT, CYNTHIA H	

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 02/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/614,040	LIN ET AL.	
	Examiner	Art Unit	
	Cynthia Britt	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-24 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-24 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 08 July 2003 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

The drawings are objected to because descriptive labels other than numerical are needed for figures 1-4. See 37 CFR 1.84(o). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Van Kirk U.S. Patent No. 6,968,485.

As per claims 1 and 13, Van Kirk teaches the claimed method for testing signals of integrated circuits (ICs), comprising the steps of: successively driving, by a first IC chip, a plurality of test patterns one at a time; receiving, at a second IC chip, and latching in the test patterns on by one; determining, by the second IC chip, whether a currently latched test pattern is correct; if at least an error bit occurs in the currently

latched test pattern, the second IC chip indicating that there exists noise interference in a signal trace corresponding to the error bit; and repeating the above steps until the first IC chip finishes driving the test patterns (Abstract, Figure 1, 155).

As per claims 2 and 14, Van Kirk teaches the test patterns are at least divided into three types including a ground bounce type, a power bounce type and a heavy load type (column 11 line 32 and column 20 line 50-60).

As per claims 3 and 15, Van Kirk teaches the step of: if the currently latched test pattern is incorrect, the second IC chip adjusting a reference voltage level in accordance with the type of the corresponding test pattern to change an input threshold of the second IC chip (column 1 line 39-40, column 2 line 12-15, column 2 line 55-60, column 3 line 40-45).

As per claims 4 and 16, Van Kirk teaches the reference voltage level is decreased to lower the input threshold of the second IC chip if the corresponding test pattern belongs to the power bounce type (Figure 15, column 4 line 60, column 12 line 36-45, column 14 line 63, column 13 line 1-20).

As per claims 5–7 and 17-19, Van Kirk teaches the techniques of testing reference voltages as noted in claims 2, 3, and 4. (Figure 15, column 4 line 60, column 12 line 36-45, column 14 line 63, column 13 line 1-20).

As per claims 8 and 20, Van Kirk teaches the step of: adjusting a driving capability of a pin relative to the error bit for the first IC chip to change the pin's output timing (Abstract, Figure 1, 155).

As per claims 9 and 21, Van Kirk teaches the driving capability of the pin relative to the error bit is increased to advance the pin's output timing for the first IC chip (column 3 line 40-45).

As per claims 10 and 22, Van Kirk teaches the driving capability of the pin relative to the error bit is decreased to delay the pin's output timing for the first IC chip (column 4 line 60, column 12 line 36-45).

As per claims 11 and 23, Van Kirk teaches the method of claim 8 wherein the output timing is changed in a unit of 150 ps at a time when adjusting the pin's driving capability for the first IC chip (column 3 line 10-20).

As per claim 12 and 24, Van Kirk teaches the output timing is adjusted by changing an internal register setting of the first IC chip (Figures 2A and 2B).

Conclusion

"Validation And Test Issues Related to Noise Induced by Parasitic Inductances of VLSI Interconnects" by Sinha et al. IEEE Transactions on Advanced Packaging Publication Date: Aug. 2002 Volume: 25 Issue: 3 pages 329 – 339, INSPEC Accession Number:7496558

This paper shows the results of studies of noise induced by various combinations of parasitic capacitances and inductances. Interconnects are simulated with parameters obtained from a 0.18 /spl mu/m process. The four kinds of noise addressed are (i) crosstalk pulse; (ii) crosstalk speedup and slowdown; (iii) oscillatory noise; (iv) combination of oscillatory noise and crosstalk pulse. The crosstalk effects induced by a

combination of mutual capacitance and mutual inductance can be larger than those induced by mutual capacitance alone, even if capacitive crosstalk dominates. For certain interconnects that are capacitively and inductively coupled, transitions in the same direction on an aggressor and victim line can cause speedup or slowdown, depending on timing parameters. A similar observation holds for transitions in opposite directions. We also observe that oscillatory noise can combine with crosstalk pulse under certain skew conditions and give rise to a large magnitude of noise. We show that inductance induced noise can be a problem in medium length interconnects. Because such interconnects can occur in combinational logic blocks, the generation of suitable vectors for test and validation of such logic blocks is of concern.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 571-272-3815. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Cynthia Britt

Cynthia Britt
Examiner
Art Unit 2138